A NEW MICROWAVE HIGH POWER TRANSISTOR (STATIC INDUCTION TRANSISTOR)

Yasuya KAJIWARA, Kenji HORIKIRI, Yoshinori YUKIMOTO,
Genshiro NAKAMURA, and Masao AIGA

Semiconductor Laboratory, Mitsubishi Electric Corporation.

4-1 Mizuhara, Itami, Hyogo 664 Japan.

ABSTRACT

A high power transistor at microwave frequency has been realized by multi-chips of static induction transistor. An output power of 100 W at 1 GHz was obtained by good design of thermal balance and improvement of packaging. A gain of 2.2 dB and a drain efficiency of 42 % was obtained at output power of 100 W. The linear gain was 3.6 dB.

INTRODUCTION

There are increasing demands for alternatives to electron tubes in the microwave frequency ranges. Since the invention by prof.Nishizawa several years ago,[1] the static induction transistor (SIT) has made a great stride for the progress in power and frequency characteristics. And now it reaches to the bipolar transistors with respect to the power in microwave frequency as well as low frequency. The reasons for this success will be derived from the follwing merits of the SIT.

(1) The operation of SIT is characterized by the majority carrier injection and the carrier drift by electric field. The drift velocity of carriers is so high that the SIT is suitable for high voltage operation at high frequency.

(2) Negative temperature coefficient of drain current saves the SIT from thermal run away. The SIT is stable at high power operation.

We already reported 10W and 20W SITs operated at 1 GHz.[2,3] Now, we obtained an output power of 100 W by multi-chips operation and verified the SIT to be an excellent and promising device as a high power transistor operating at microwave frequency.

In the following, the method of power combination of SITs and the improved designs for the chips and package are repoted.

DESIGN AND FABRICATION

The fundamental structure of the SIT, shown in Fig.1, is similar to a vertical J-FET.[3] However, the operation mechanism is different from each other. SIT has short channels which are almost pinched off by the built in potential of PN^+ junction. Electrons are injected from N^+ source region into the depleted drain region over the potential barrier of which height is controlled by gate and drain voltage.

From the operation mechanism of SIT, an equivalent circuit for small signal operation at high frequency is expressed, as shown in Fig.2. Intrinsic resistance appeared in the equivalent circuit of FET was ignored because of the channel depletion in SIT.[4]

The unilateral power gain U and the maximum stable power gain MSG were approximately expressed by following equations,

$$U \cong \frac{Gm^2}{4\omega^2\{(C_G+C_{DG})(\zeta_s+\zeta_g)G_D+C_{DG}(2\zeta_s+\zeta_g)Gm\}} \quad (1)$$

$$MSG \cong \frac{Gm}{\omega C_{DG}} \quad (2)$$

Where, $\zeta_s = R_S(C_G+C_{DG})$, $\zeta_g = R_G(C_G+C_{DG})$ and $\omega = 2\pi f$. f is a operating frequency.

Because $\mu(=Gm/G_D)$ is around 10, the effect of C_{DG} on U is about 10 times larger than that of C_G. The expression of MAG was rather complicated and difficult to get the images of the effect of individual parameters on MAG. For an example, Fig.3 shows the U, MAG and MSG obtained by the numerical calculation.

Fig.3 also shows that the source inductance L_S is drastically effective on MAG, but negligibly effective on U and MSG. Inductances of L_G and L_D are little effective on these values.

From the analysis of the equivalent circuit, special attention shoud be made to increase Gm and to decrease C_{DG} and L_S. Another cares to be paid for high power operation were to have a high breakdown voltages BV_{DG} and BV_{SG} and effective thermal dispersion.

The following design principles were taken into consideration for the fabrication of SIT.

(1) In an SIT, Gm increases with the impurity concentration.[3] Considering the breakdown voltage, the impurity concentration was optimized.

(2) C_{DG} is proportional to the active area of gate and source regions. To reduce C_{DG}, it is necessary to make the gate and source regions as fine as possible. A self-aligning process employing Si_3N_4 film was used.[3]

CH1355-7/78/0000-0380$00.75

(3) The reduction of L_S value is concerned with the assembly of the chips. A new package was designed to obtain a low L_S value and the bonding technique was improved to minimize the length of source leading wires by connecting at the both side of the chips, as shown in Fig.4.

(4) Thermal dispersion technique is one of the most important design problems. To obtain the thermal balance on the SIT, the active regions were dispersed with several cells, as shown in Fig.5.

EXPERIMENTAL RESULTS

Characteristics of an SIT chip

I-V characteristic of an SIT is triode-like.[3] Typical characteristics of a fabricated SIT are shown in table 1.

BV_{DG} (V)	95
BV_{SG} (V)	40
Gm (mS)	150
G_D (mS)	20
C_{DG} (pF)	5
C_G (pF)	9

Table 1. Typical characteristics of an SIT chip.

From small signal scattering parameters, U and MAG at 1 GHz were about 10 dB and 5 dB, respectively. MSG was 15 dB at 0.1 GHz and decreased with 3 dB/octave. From equ.(1), U was estimated 15 dB at 1 GHz, when R_S and R_G were 0.1 ohms evaluated from resistance of metal leading lines. MSG was also estimated 17 dB at 0.1 GHz from equ. (2). These values nearly coincided with the measured values.

For high power operation, the thermal balance on a chip is very important. The temperature distribution on the surface of a chip was relatively uniform and the temperature difference in active region was about 10 °C at power dissipation of 20 W, as shown in Fig.6. The amplifying output power was 20 W with gain of 4 dB at 1 GHz.

Multi-chips operation

At 2 chips operation, U and MAG were 10 dB and 4 dB at 1 GHz, respectively, as shown in Fig.7. S_{11} and S_{22} became inductive at higher frequency than 1GHz, as shown in Fig.8.
It is considered that the gate and drain leading wires make S_{11} and S_{22} inductive, by using larger package than that of one chip. However, the decrease of MAG was a little, by prevention of increasing L_S.
The power amplification characteristics of multi-chips operation are shown in Fig.9. By 2 chips parallel operation, the output power was 51 W with gain of 3 dB at 1 GHz. The applied voltages at drain and gate were 80 V and -14 V, respectively. The drain efficiency was 56 % and the amplifier operated at near B class.

At 4 chips operation, the output powers of a pair of 2 chips were combined, because the input and output impedances got too low. After heightening each impedance, input and output terminals were connected. The output power of 100 W was obtained with gain of 2.2 dB and efficiency of 42 %.

From above results, it has been verified that SIT is suitable for high power microwave transistor. In near future, the gain of SIT will be improved by progress of fine patterning and power combination techniqes.

CONCLUSION

Multi-chips operation of SIT has been well succeeded by improvement of packaging. At 2 chips operation, the output power of 51 W with gain of 3 dB and efficiency of 56 % was obtained. At a pair of 2 chips operation, the output power of 100 W with gain of 2.2 dB and efficiency of 42 % was obtained at 1 GHz.

ACKNOWLEDGEMENT

The authors are grateful to professor J.Nishizawa for many helpful discussions. They wish to thank to Dr. T.Kitsuregawa and Dr. K.Shirahata for their encouragements in this work.

REFERENCES

1) J.Nishizawa et al ; " Field Effect transistor versus Analog transistor (Static Induction Transistor)", IEEE Trans. ED-22, pp 185-197 (1975)

2) Y.Kajiwara et al; "High Power Microwave Static Induction Transistor",IEEE MTTs 1977 International Microwave Symposium, pp 281-284

3) Y.Kajiwara et al: "High Power Static Induction Transistor for Microwave Operation", 7th European Microwave Conference, 1977,pp629-633

4) P.Wolf ; "Microwave properties of Schottky barrier Field Effect Transistors", IBM. J. Res. Develop. 14 , pp 125-141, (1970)

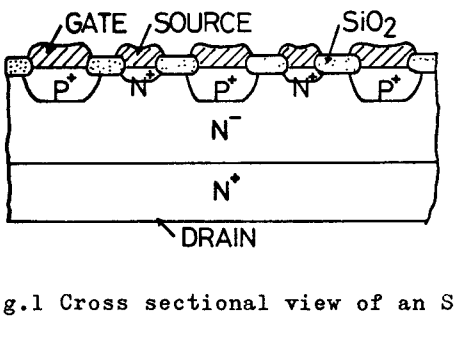

Fig.1 Cross sectional view of an SIT.

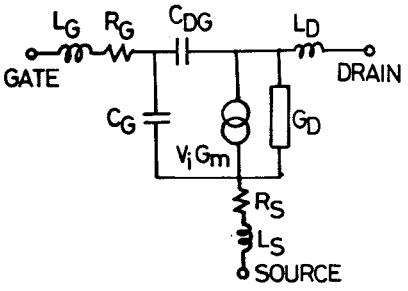

Fig.2 Equivalent circuit of an SIT

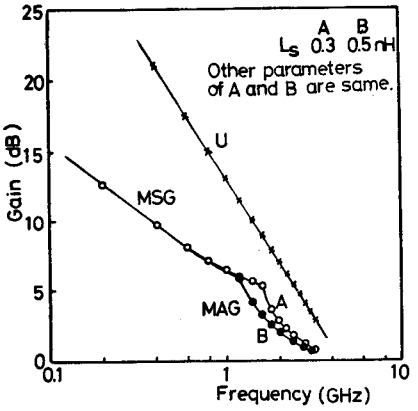

Fig.3 Calculated U, MSG and MAG from the equivalent circuit.

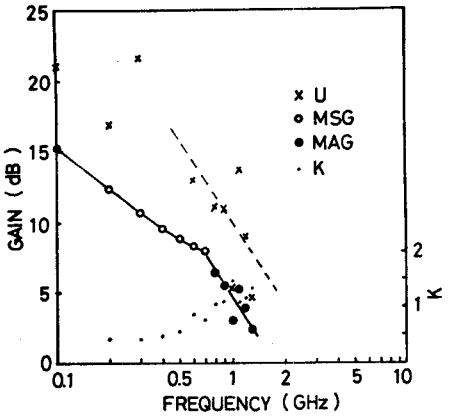

Fig.7 U, MSG and MAG of a tow chip device.

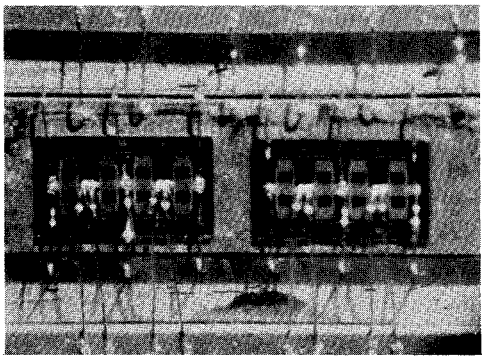

Fig.4 Assembled SIT.

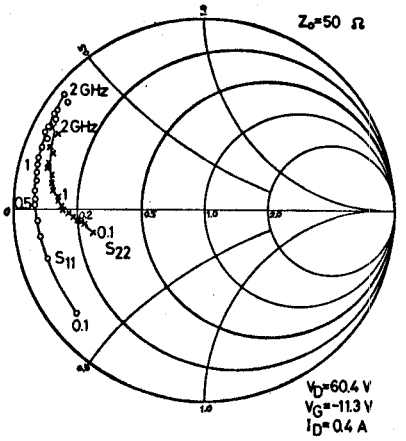

Fig.8 S_{11} and S_{22} characteristics of a tow chip SIT device.

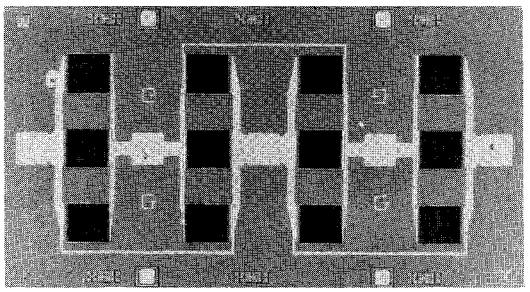

Fig.5 Top viw of an SIT.

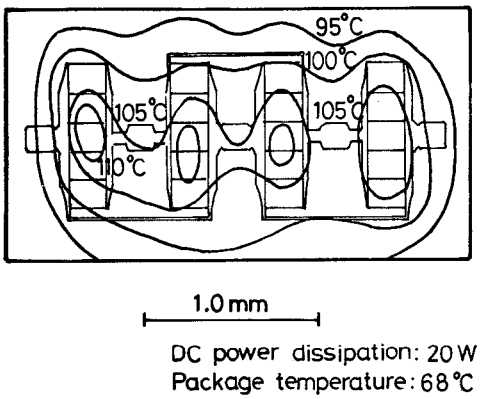

Fig.6 Temperature distribution on an SIT chip.

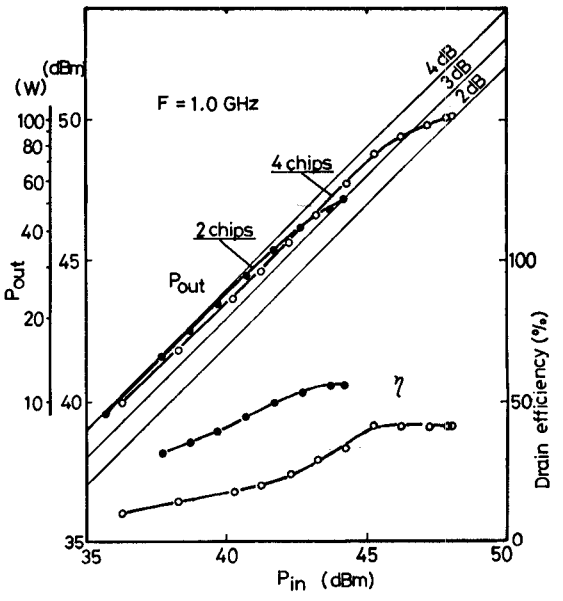

Fig.9 Amplification characteristics of multi-chips SITs.